Amendments to the Claims:

The following listing will replace all prior listing of claims in the application.

Listing of Claims:

1. (Currently amended) A semiconductor component with trench isolation for defining active regions in a semiconductor substrate ~~(1, 2, 3)~~, the trench isolation ~~(STI, TTI) having~~ comprising:

a deep isolation trench with a covering insulation layer ~~(10, 11)~~, a side wall insulation layer ~~(6)~~, and an electrically conductive filling layer, which is electrically connected to a predetermined doping region of the semiconductor substrate in a bottom region of the isolation trench~~;~~, and

~~characterized by~~ further comprising:

a trench contact ~~(DTC)~~, which ~~has~~ comprises a deep contact trench with a side wall insulation layer ~~(6)~~ and an electrically conductive filling layer ~~(7)~~, which is likewise electrically connected to the predetermined doping region of the semiconductor substrate ~~(1, 2, 3)~~ in a bottom region of the contact trench.

2. (Currently amended) The semiconductor component ~~as claimed in patent~~ of claim 1, wherein the covering insulation layer ~~(10, 11)~~ is formed essentially below a ~~semiconductor substrate~~ surface of the semiconductor substrate and within the isolation trench.

3. (Currently amended) The semiconductor component ~~as claimed in patent~~ of claim 1 ~~or 2~~, wherein the trench isolation ~~(STI, TTI)~~ and the trench contact ~~(DTC)~~ have a larger depth than an associated depletion zone in the semiconductor substrate ~~(1, 2, 3)~~.

4. (Currently amended) The semiconductor component ~~as claimed in one of patent claims~~ of claim 1 ~~to 3~~, wherein the trench isolation ~~(STI)~~ ~~has~~ further comprises a widened, shallow isolation trench at a surface of the semiconductor substrate ~~surface~~ configured for ~~the purpose of~~ filling non-active regions.

5. (Currently amended) The semiconductor component ~~as claimed in one of patent claims~~ of claim 1 ~~to 4~~, wherein the predetermined doping region ~~constitutes~~ comprises a doping well ~~(2)~~ ~~of~~ comprising a multiple well structure.

6. (Currently amended) The semiconductor component ~~as claimed in one of patent claims~~ of claim 1 ~~to 5~~, wherein the semiconductor substrate ~~(1, 2, 3) has~~ comprises Si, the covering insulation layer and side wall insulation layer ~~(6, 10, 11) has~~ comprise SiO_2, and the filling layer ~~(7) has~~ comprises highly doped polysilicon.

7. (Currently amended) A method for fabricating a semiconductor component ~~with~~ having trench isolation ~~having the following steps~~ comprising:

a) ~~Preparation of~~ preparing a semiconductor substrate ~~(1, 2, 3) with~~ having at least one predetermined doping region ~~(2)~~;

b) ~~Formation of~~ forming deep trenches ~~(T) as far as~~ to the predetermined doping region ~~(2) for the purpose of realizing~~ configured for at least one trench isolation ~~(STI, TTI)~~ and a trench contact ~~(DTC)~~;

c) ~~Formation of~~ forming a side wall insulation layer ~~(6) at~~ on the side walls of the deep trenches ~~(T)~~;

d) ~~Formation of~~ forming an electrically conductive filling layer ~~(7)~~ in the deep trenches ~~(T)~~;

e) ~~Removal of~~ removing at least the electrically conductive filling layer ~~(7)~~ in the upper region of the trenches for the at least one trench isolation ~~(STI, TTI) for the purpose of forming~~ to form shallow trenches ~~(ST)~~; and

f) ~~Formation of~~ forming a covering insulation layer ~~(10, 11)~~ in the shallow trenches ~~(ST)~~ of the trench isolation ~~(STI, TTI)~~.

8. (Currently amended) The method ~~as claimed in patent~~ of claim 7, wherein~~, in step a),~~ preparing a semiconductor substrate having at least one predetermined doping region comprises forming one of a double or triple well structure ~~is formed~~ in the semiconductor substrate.

9. (Currently amended) The method ~~as claimed in patent~~ of claim 7 ~~or 8~~, wherein~~, in step b),~~ forming ~~the~~ deep trenches ~~(T) are formed~~ comprises ~~using~~ forming a first hard mask layer ~~(5) by means of an anisotropic~~ and anisotropically etching ~~method in~~ the semiconductor substrate.

10. (Currently amended) The method ~~as claimed in one of patent claims~~ of claim 7 ~~to 9~~, wherein~~, in step c),~~ forming a side wall insulation layer comprises ~~a thermal oxidation is carried out in order~~ thermal oxidation to form a trench insulation layer and ~~an anisotropic~~ anisotropically etching ~~method is carried out in order~~ the trench insulation layer to remove a bottom region of the trench insulation layer.

11. (Currently amended) The method ~~as claimed in one of patent claims~~ of claim 7 ~~to 10~~, wherein~~, in step d),~~ forming an electrically conductive filling layer comprises forming a highly doped semiconductor material ~~(7)~~ having the same conduction type ~~(n)~~ as the predetermined doping region ~~(2) is deposited~~.

12. (Currently amended) The method ~~as claimed in one of patent claims~~ of claim 7 ~~to 11~~, wherein, in step e), ~~in order to realize a widened trench isolation (STI)~~, forming shallow trenches further comprises removing ~~the conductive filling layer (7),~~ the side wall insulation layer ~~(6)~~ and adjoining regions of the semiconductor substrate ~~(1, 2, 3) are removed~~ in the upper region of the deep trenches ~~(T)~~ to form widened trench isolation structures.

13. (Currently amended) The method ~~as claimed in one of patent claims~~ of claim 7 ~~to 12~~, wherein~~, in step e),~~ forming shallow trenches comprises ~~in order to realize a narrow trench isolation (TTI),~~ removing only the conductive filling layer ~~(7)~~ with or without the side wall insulation layer ~~(6) is removed~~ in the upper region of the trenches to form narrow trench isolation structures.

14. (Currently amended) The method ~~as claimed in one of patent claims~~ of claim 7 ~~to 12~~, wherein~~, in step f),~~ forming a covering insulation layer ~~an oxidation is carried out in order~~ comprises one of oxidizing to form a first covering insulation partial layer ~~(10) and/~~or ~~a deposition is carried out in order~~ depositing to form a second covering insulation partial layer ~~(11)~~ in the shallow trench ~~(ST)~~, or both oxidizing and depositing.